

CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A method of forming bitline contacts, the method comprising:

forming gate conductor lines with a capping layer on a substrate;

depositing an oxide layer over the capping layer;

forming a bitline contact line mask over portions of the oxide layer;

etching the bitline contact line mask to the capping layer and between the gate conductor lines stopping at the substrate;

depositing a silicon layer on the substrate between the conductor lines and non etched portions of the oxide layer;

depositing a bitline layer on the silicon layer;

masking and etching portions of the bitline layer; and

depositing metal over the silicon layer and on sides of non etched portions of the bitline layer to form left and right bitlines.

1 2. The method of claim 1, wherein a layer of
2 BoroPhosphoSilicate Glass (BPSG) is deposited over
3 the capping layer prior to the deposition of the
4 oxide layer.

1 3. The method of claim 2, further comprising
2 annealing the BPSG layer.

1 4. The method of claim 3, further comprising
2 planarizing the BPSG layer to below tops of the gate
3 conductor lines.

1 5. The method of claim 1, wherein the oxide layer
2 is a TEOS layer.

1 6. The method of claim 5, further comprising
2 planarizing the TEOS layer prior to forming the
3 bitline contact line mask.

1 7. The method of claim 1, further comprising
2 forming spacers between adjacent gate conductor
3 lines.

1 8. The method of claim 7, further comprising
2 depositing a layer of BoroPhosphoSilicate Glass
3 (BPSG) over the capping layer wherein the etching of
4 the oxide and BPSG selective to the capping layer

5 and selective to the spacers.

1 9. The method of claim 1, wherein the silicon layer
2 is an n+ amorphous/polysilicon layer.

1 10. The method of claim 9, wherein the n+
2 amorphous/polysilicon layer is selectively etched or
3 polished back to the oxide layer, the oxide layer
4 being a TEOS layer.

1 11. The method of claim 10, further comprising
2 etching the n+ amorphous/polysilicon layer to below
3 tops of the gate conductor lines and below the oxide
4 layer.

1 12. The method of claim 11, further comprising
2 planarizing the bitline layer, the bitline layer
3 being a TEOS layer.

1 13. The method of claim 1, wherein the etching of
2 the bitline stops at the non etched portions of the
3 oxide layer.

1 14. The method of claim 1, wherein the oxide layer
2 is etched to the silicon layer selective to the
3 capping layer encapsulating the gate conductor
4 lines.

1 15. The method of claim 1, further comprising
2 forming insulating sidewalls on the gate conductor
3 lines.

1 16. The method of claim 15, wherein the insulating
2 materials is silicon nitride.

1 17. The method claim 16, further comprising
2 depositing a conformal silicon nitride layer on the
3 gate conductor lines and active areas and isolation
4 areas between the active areas.

1 18. The method of claim 1, wherein an isotropic dry
2 etch is used to recess the silicon layer to below a
3 level of the capping layer.

1 19. A bitline contact for a vertical DRAM array,
2 comprising:
3 gate conductor lines formed on a substrate;
4 a polysilicon layer formed between the gate
5 conductor lines;
6 an oxide layer formed over at least one of the
7 gate conductor lines; and
8 metal formed over the gate conductor lines on
9 opposing sides of the oxide layer thereby forming a
10 left bitline and a right bitline, wherein the left

11 and right bitlines are vertically non-twisted
12 between bitline levels.

1 20. The bitline contact of claim 19, further
2 comprising an insulator layer formed between the
3 gate conductor lines and the polysilicon layer.

1 21. The bitline contact of claim 19, wherein the
2 polysilicon layer is an N+ amorphous/polycrystalline
3 silicon layer.

1 22. The bitline contact of claim 19, wherein the
2 oxide layer is a TEOS oxide.

1 23. The bitline contact of claim 19, further
2 comprising spacers between two adjacent gate
3 conductor lines of the gate conductor lines.

1 24. The bitline contact of claim 23, further
2 comprising a layer of BoroPhosphoSilicate Glass
3 (BPSG) and a topping oxide layer formed over the
4 spacers.

1 25. The bitline contact of claim 24, wherein the
2 left and right bitlines are formed partially over
3 the topping oxide layer.

1 26. The bitline contact of claim 24, wherein the
2 topping oxide layer is a TEOS layer.

1 27. The bitline contact of claim 19, wherein the
2 polysilicon layer is formed below tops of the gate
3 conductor lines.

1 28. The bitline contact of claim 27, wherein the
2 right and left bitlines are partially formed below
3 the tops of the gate conductor lines.